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Effects of Carbon Nanotube Diameter and Gate-Dielectric Constant on 6T, 8T and 10T CNTFET SRAM: A MATLAB-Based Modelling Study

***[1]Busari Kehinde Abdulsemiu and [1]Mutari Hajara Ali**

[1]Department of Physics, Federal University, Gashua.
[2]Department of Physics, Bayero University, Kano.

*Corresponding authors' email: kehindesemiu@fugashua.edu.ng
Orcid id: https://orcid.org/0000-0001-8612-8459

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ABSTRACT
This paper evaluates the effect of Carbon nanotube (CNT) diameter and gate-dielectric constant (k) on the performance of CNT Field Effect Transistor (CNTFET) Static Random-Access Memory (SRAM) cell topologies (6T, 8T, 10T and 10T modified). Current, Capacitance and Voltage Transfer characteristics (VTCs) models were derived from Cadence-Stanford CNTFET compact model and implemented in MATLAB scripting environment. The evaluation is carried out for all specified SRAM cells with the resulting analytical models by varying CNT diameter (D_{CNT}) and gate-dielectric constant (k) on key SRAM performance metrics, including read/write delay, power consumption, Power-Delay Product (PDP), Energy-Delay Product (EDP) and Static Noise Margin (SNM). Results indicate a 59.5% and 63.4% reduction in read and write delay using silicon dioxide (SiO_2) as a gate-dielectric material (k=3.9) within a CNT diameter range of 1.0179-1.644nm for 8T SRAM cell respectively. Furthermore, at 1.95575nm and dielectric constant range of 3.9-30, there is 1.33% increase in power consumption, alongside reductions of 63.9% in write delay, 64.6% in read delay, 63.42% in PDP and 86.8% in EDP respectively. Relative to cadence, this implies substantial improvements with percentage error range of 15-50% across the evaluated performance metrics. Among the evaluated topologies, modified 10T SRAM exhibits high stability, low delay and PDP with increase of 0.97% in SNM, reductions of 64.4% in delay and 99% in PDP/EDP. These findings demonstrate that the analytical framework can effectively capture parameter-dependent performance trends and support analysis and optimization of high-speed, low-power, energy efficient and stable SRAM architectures for future nanoscale memory applications.

Keywords: Memory, SRAM, CNTFET, Topology, PDP/EDP

INTRODUCTION

It is obvious that the growing performance of memory technology is advancing through improved speed, energy efficiency, scalability and stability. However, memory being a computer hardware component, comprises semiconductor-based integrated circuits that provide high-speed data access to the Central Processing Unit (CPU) (Zhu & Qiang, 2012; Zlatanov, 2016; Busari & Mutari, 2026). Static Random Access Memory (SRAM) is indispensable and widely used as cache memory to enable high speed, low latency, and reliable data retention for modern processors, portable electronics, IoT devices, and other battery-powered systems (Zlatanov, 2016; Yalla & Nanda, 2019; Maity et al., 2020; Pal et al., 2022; Fuad et al., 2025a; Sharma & Kumar, 2025). As estimated by International Technology Roadmap for Semiconductors (ITRS), SRAM dominates 90% chip area of System-on-Chip (SoC) designs (modern processors) with a substantial influence on overall system performance (Pal & Islam, 2016; Nayak et al., 2018; Nayak et al., 2020; Gupta & Dasgupta, 2019). In that context, SARM remain significant for embedded applications with an essential role in Very Large-Scale-Integration (VLSI) systems (Nayak *et al.*, 2020). At nanoscale dimension, Carbon Nanotube Field Effect transistors (CNTFETs) become an alternative to other types of semiconductor-based transistors (Fei, 2024). CNTFETs play a crucial role in low power and energy-efficient SRAM designs due to their high carrier mobility (high Ion/Ioff ratio), ballistic transport and quantum mechanical effects influencing device performance for ideal memory applications (Natori et al., 2005; Lázaro et al., 2006; Sinha et al., 2014; Rastogi et al., 2015; Nidhi & Prashant, 2019; Jahanirad & Hosseini, 2021; Fuad et al., 2023; Fuad et al., 2024). Due to process variation that arises from one transistor to another during chip manufacturing, device performance is considered an important factor in CNTFET-based SRAM design. In this case, SRAM performance becomes sensitive to parameter variation such as threshold voltage-shift, gate oxide thickness, CNT diameter and dielectric constant of gate-dielectric material (Sinha & Chaudhury, 2012). Topology being a circuit-level factor, accounts for transistor-level schematic of a single memory cell and it is primarily categorized by the number, arrangement, interconnection of transistors and its circuit components in a CNTFET SRAM such as 6T, 7T, 8T, 9T and 10T. The connectivity of these transistors with the reading and writing of data in a memory cell is also crucial to SRAM architectures.

Despite the potential of CNTFETs for low power SRAM applications, their performance is highly sensitive to CNT diameter and gate-dielectric constant with their effect varying across different SRAM cell topologies. Variations in these parameters influence overall SRAM's performance including delay, power consumption, stability and energy efficiency metrics. However, this performance has been predominantly investigated through transistor-level simulations with limited analytical evaluation. This emphasizes the need for a MATLAB-based systematic analytical framework that

evaluates Cadence performance trends on these parameter-dependent effects across CNTFET-based SRAM topologies.
Zhang and Delgado-Frias (2012) investigated CNTFET-based 8T SRAM using metallic-CNT-tolerant and metallic-CNT-free approaches, achieving comparable SNM while reducing CNT count and write delay to 36.5% and 10.9%, respectively. Pasandi et al. (2015) reported improved read and write noise margins (RNM/WNM) in a 10T CNTFET SRAM, with a 13% reduction in power consumption compared with other topologies. In Devi et al. (2021) improvements of 37.44% in power consumption and 27.55% in stability, alongside a 13% reduction in delay was demonstrated. Valluria and Musala (2022) comparatively evaluated 8T, 9T, and 10T CNTFET SRAMs, reporting improved RNM/WNM and lower power consumption relative to conventional 6T/7T cells, with the 7T topology achieving 30% and 36% improvements in power consumption and WNM, respectively. More recently, Fuad and Nayan (2026) evaluated 6T, 8T, 10T, and modified-10T CNTFET SRAMs, reporting 13.08%, 12.13%, and 11.20% reductions in write delay, read delay, and PDP, respectively. The modified-10T cell achieved a write delay of 4.8 ps, PDP of 870.03 zJ, and SNM of 462.21 mV. Despite these advances, a comprehensive analytical evaluation of CNTFET-based SRAM topologies under varying device and material parameters remains limited. This motivates further investigation of SNM, delay, power consumption, and energy-efficiency metrics to identify topology–parameter trade-offs for high-performance and low-power SRAM design.
Therefore, this study aims to evaluate the effect of CNT diameter and dielectric constant on the performance of CNTFET-based SRAM cell topologies using MATLAB-based analytical models derived from Stanford-Cadence 32nm simulations. The primary objective is to significantly improve the performance of four different CNTFET-based SRAM cell topologies (6T, 8T, 10T and 10T modified) and identify the SRAM cell topology with the optimal delay, power consumption, PDP, EDP and SNM under CNT diameter and gate-dielectric constant variations.

Background Theory

In this section, we introduce the structures and theoretical models needed for the performance evaluation of CNTFET-based SRAM cell topologies under the influence of CNT diameter and dielectric constant variation. These models are established on the theory of quantum mechanical model involving ballistic transport equations, chirality of CNTs, energy efficiency parameters and stability characteristics.

Device Compact Model

The CNTFET model is a compact model derived from Stanford-Cadence simulation at 32nm technology node and it is crucial for the MATLAB-based analysis of SRAM's performance. The compact model is a SPICE-compatible model of Cadence Virtuoso nanoscale circuit simulation which incorporates quasi-ballistic carrier transport, quantum and parasitic capacitance, Schottky resistance and scattering mechanisms. To ensure accurate prediction of the device behavior, we consider key design parameters such as CNT diameter and gate-dielectric constant influencing threshold voltage (V_{TH}), drive/on current (Ion), switching speed and stability across different SRAM cell topologies. In this regard, the drive current model equations are given by Equations (1&4) (Natori, 1994; Murotiya et al., 2014; Nayan, 2019).
In the case of drain-source on-current for thermionic emission and saturation region we have Equation (1-4),

$$I_{DS} = N_{CNT}.\frac{4qk_BT}{h} ln\left[1 + exp\left(\frac{2qV_{GS}-E_g}{2k_BT}\right)\right] \quad (1)$$

$$I_{DS} = B\mu_n C_{eff}\frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{{V_{DS}}^2}{2}\right](1 + \lambda V_{DS}) \quad (2)$$

$$I_{DS} = \frac{1}{2}B\mu_n C_{eff}\frac{W}{L}(V_{GS} - V_{TH})^{\alpha} v_{sat}(1 + \lambda V_{DS}) \quad (3)$$

$$I_{on} = B\mu_n C_{eff}\frac{W}{L}(V_{DD} - V_{TH})^{\alpha} \quad (4)$$

For CNT diameter and dielectric constant dependent case across different topologies, we have Equation (5&6) (Maleknejad et al., 2014; Tiwari et al., 2015; Yang et al., 2020),

$$I_{on} = I_0\left(\frac{D}{D_0}\right)^{\alpha} \quad (5)$$

$$I_{on} = I_0\left(\frac{D}{D_0}\right)^{\alpha}\left(\frac{k}{k_0}\right)^{\beta} \quad (6)$$

$$E_g = \frac{0.84}{D_{CNT}}(eV) \quad (7)$$

$$V_{TH} = \frac{a \times V_{\pi}}{\sqrt{3}\, q\, D_{CNT}} = \frac{E_g}{2q} \cong \frac{0.42}{D_{CNT}\,(nm)} \quad (8)$$

$$D_{CNT} = \frac{a\sqrt{r^2+s^2+rs}}{\pi} \quad (9)$$

$$\theta = \tan^{-1}\frac{\sqrt{3}r}{r+2s} \quad (10)$$

Where the numerator part of Equation (9) is the Chirality, V_{DD}, V_{GS}, V_{DS}, μ_n , λ, $N_{CNT,}$ q, K_B, T, h, Ceff, E_g, B, W, L, D_{CNT}, r, s, α, β, k, q, a, Vπ and Θ are supply voltage, gate-source voltage, drain-source voltage, carrier mobility, leakage growth factor, CNT number, electronic charge, Boltzmann constant, temperature, Planck's constant, effective capacitance, energy bandgap, ballistic factor, gate width, channel length, CNT diameter, chirality vectors, velocity saturation factor, leakage degradation factor, gate-dielectric constant, electronic charge, graphene grid constant (0.249 nm), carbon energy bond (0.3033 eV) and chiral angle respectively.

Delay Model

Propagation delay (t_d) is the time taken for a signal to travel through a circuit or logic gate (Busari & Mutari, 2026). In SRAM's operation, it is determined by charging and discharging of internal storage nodes and bitlines. It also determines the switching speed and ensures the read and write access in transistor network. However, the minimum time between the write and read operations in SRAM is determined by the operational cycle. Therefore, the delay compact model equations are given by Equations (11-17) (Deng & Wong, 2007; Sze & Ng, 2007; Taur & Ning, 2013; Fuad et al., 2025b).

$$t_d = \frac{C_{eff}V_{DD}}{I_{on}} \quad (11)$$

$$C_{eff} = C_{ox} + C_Q + C_{par} \quad (12)$$

$$C_{ox} = \frac{2\pi\varepsilon_0 k\, L}{\ln\left(\frac{2T_{ox}}{D}+1\right)} \quad (13)$$

$$C_Q = \frac{4q^2}{hv_F} \quad (14)$$

Taking note of the parasitic, oxide and quantum capacitance (Cpar, Cox, C_Q) respectively, Equation 10 becomes

$$t_d = \frac{(C_{ox}+C_Q+C_{par})V_{DD}}{I_{on}} \quad (15)$$

For the case of write and read delay we can re-write Equation (15) as

$$t_{write/read} = \frac{(C_{ox}+C_Q+C_{par})V_{DD}}{I_{on}} \quad (16)$$

For SRAM topologies, load and parasitic capacitance (C_L, C_{par}) slightly vary by calibration and Equation (16) becomes

$$t_{write/read} = F_{dT}\frac{(C_{ox}+C_Q+C_{par}+C_L)V_{DD}}{I_{on}} \quad (17)$$

Where, h, V_F, ε0, k, Tox and F_{dT} are planck's constant, fermi velocity, relative permittivity, gate-insulator relative permittivity dielectric constant, gate-oxide thickness and delay topology factor respectively. Despite same general

expression for read and write delay, their distinction still stems from separate current paths, resistances, capacitances and switching activities.

Power Consumption Model

The total power consumption (P_{total}) of a SRAM cell is the summation of leakage power (P_{leak}) and dynamic power (P_{dyn}) (Busari & Mutari, 2026). This model provides the basis for comparing the energy efficiency of CNTFET based SRAM cells topologies under diameter and dielectric constant variation. Therefore, the model is given by Equation (12-21) (Deng & Wong, 2007; Sze & Ng, 2007; Akashe et al., 2011; Taur & Ning, 2013; Kesavan & Rajeswari, 2015; Yuan & Xue, 2024).

Considering diameter and dielectric constant variation for the four SRAM topologies, the dynamic power, leakage power, short-circuit power and total power are given by Equation (18-22) respectively.

$$P_{dyn} = \alpha_{sw} f C_{eff} {V_{DD}}^2 \quad (18)$$

$$P_{leak} = I_{leak} V_{DD} \quad (19)$$

$$P_{sc} = k_{sc} I_{on} V_{DD} \quad (20)$$

$$P_{total} = F_{PT}(P_{dyn} + P_{leak} + P_{sc}) \quad (21)$$

$$I_{leak} = G.I_0 e^{\beta(D-D_{ref})} \quad (22)$$

Considering dielectric constant variation with different gate-oxide dielectrics when there is no short circuiting, the total power is re-written as

$$P_{total} = P_{dyn} + P_{leak} \quad (23)$$

Where f, I_{leak}, α_{sw}, D_{ref}, G, F_{PT} and k_{sc}, are frequency, leakage current, switching activity factor, reference diameter, Gaussian correction factor, Power topology factor and short-circuit factor respectively. All these factors are incorporated as distinct model parameters whose values are determined through calibration process with least square curve fitting using Matlab lsqcurvefit code.

Power and Energy Delay Model

The power delay product (PDP) and energy delay product (EDP) models are metrics that evaluates SRAM's energy consumption, efficiency and operating speed during switching event (read and write operations). These models play a crucial role in the determination of overall SRAM's performance. When the PDP and EDP value is low, the SRAM efficiency and overall performance will be high under diameter and gate-dielectric constant variation across different cell topologies. Therefore, to define the overall performance of CNTFET-based SRAM, under these conditions, we utilize the model equations (24-27) (Tan et al., 2012).

For diameter and dielectric constant variation on the four SRAM topologies, the PDP and EDP are given by Equation (23 and 24) respectively

$$PDP = P_{total} \times t_d \quad (24)$$

$$EDP = P_{total} \times {t_d}^2 \quad (25)$$

Combining Equations (17 and 21), we have

$$PDP = F_{PT}.F_{dT}\left(P_{dyn} + P_{leak} + P_{sc}\right)\frac{(C_{ox}+C_Q+C_{par}+C_L)V_{DD}}{I_{on}} \quad (26)$$

$$EDP = F_{PT}.{F_{dT}}^2\left(P_{dyn} + P_{leak} + P_{sc}\right)\left(\frac{(C_{ox}+C_Q+C_{par}+C_L)V_{DD}}{I_{on}}\right)^2 \quad (27)$$

To determine the efficiency of the SRAM cell topologies, we have the percentage variation in each performance metrics (Xvar) relative to the reference diameter or dielectric condition (Xref) in Equation (28)

$$\Delta X = \frac{X_{var}-X_{ref}}{X_{ref}} \times 100\% \quad (28)$$

Static Noise Margin (SNM)

The Voltage Transfer Characteristics (VTCs) of two cross-coupled inverters result in two-lobed curve called a "butterfly curve" and it is used to determine the SNM (Singh et al., 2014; Rao et al., 2023). Therefore, SNM is defined as the length of the side of the largest square that can be embedded inside the lobes of the butterfly curve. This is a measure of SRAM's stability expressed in milli-Volts (mV) and ensures the maximum DC noise voltage required to flip its state. Therefore, higher SNM signifies great stability of SRAM cell topologies and it is given by Equation (29) (Shilpi et al., 2011)

$$SNM = \frac{V_{out}-V_{in}}{2} \quad (29)$$

To ensure and convert 45-degree rotation of the cross-coupled inverters from their VTCs through interpolation at common Y with input voltage (Vin) and output voltage (Vout), we have Equation (30-32),

$$X_1 = \frac{V_{in}-V_{out1}}{\sqrt{2}}, \quad Y_1 = \frac{V_{in}+V_{out1}}{\sqrt{2}} \quad (30)$$

$$X_2 = \frac{V_{out2}-V_{in}}{\sqrt{2}}, \quad Y_2 = \frac{V_{out2}+V_{in}}{\sqrt{2}} \quad (31)$$

$$SNM = \max_Y |X_1(Y) - X_2(Y)| \quad (32)$$

To estimate SNM against VTC butterfly curve with the specified angle rotation, Equation (32) becomes

$$SNM = \frac{\max_Y |X_1(Y) - X_2(Y)|}{\sqrt{2}} \quad (33)$$

To validate and compare the analytical model with Cadence/Spectre simulation on each performance metric for all SRAM cell topologies, we have the percentage error given by

$$\%\ Error = \left|\frac{X_{Matlab}-X_{Cadence}}{X_{Cadence}}\right| \times 100\% \quad (34)$$

The Structures of CNTFET and Its SRAM Topology

Figure 1, 2 & 3 show CNTFET in single walled structure, rolling pattern of the graphene sheets, 2-D structure and cell topologies. CNTFET uses carbon nanotube as a conduction channel and it exhibits reduced defect formation due to their quasi-1D structure but prolonged cycling can cause electromigration, dielectric trapping and breakdown particularly with high-k gate insulators. This quasi-1D structures also allows near ballistic transport at nanoscale regime, enhancing on-state current and switching speed of the device. The geometric arrangement of carbon atoms when graphene sheet is rolled into a nanotube defines its electronic behavior (metal or semiconductor) (Liu et al., 2011). This behavior is called chirality and it is associated with the CNT diameter (D_{CNT}) and threshold voltage (V_{TH}) expressed in device compact models' section (Fuad et al., 2023; Sharma & Kumar, 2025). The specified gate-dielectric materials utilized in the CNTFET are SiO_2 (k = 3.9), Al_2O_3 (k ≈ 11), $HfSiO_4$ (k ≈ 16), HfO_2 (k ≈ 25), ZrO_2 (k ≈ 30), whereas the experimentally attainable tube diameters range for semiconducting single-walled CNTs is 1.0179–1.95575 nm (Kumari et al., 2019). In figure 3, the circuit-level transistor schematic is demonstrated with CNTFET SRAM cell topologies such as 6T, 8T, 10T and 10T (Modified).

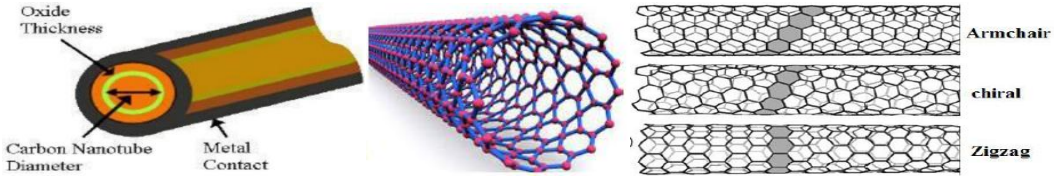


Figure 1: Single Walled CNT (Khoder et al., 2020; Tijjani et al., 2020)

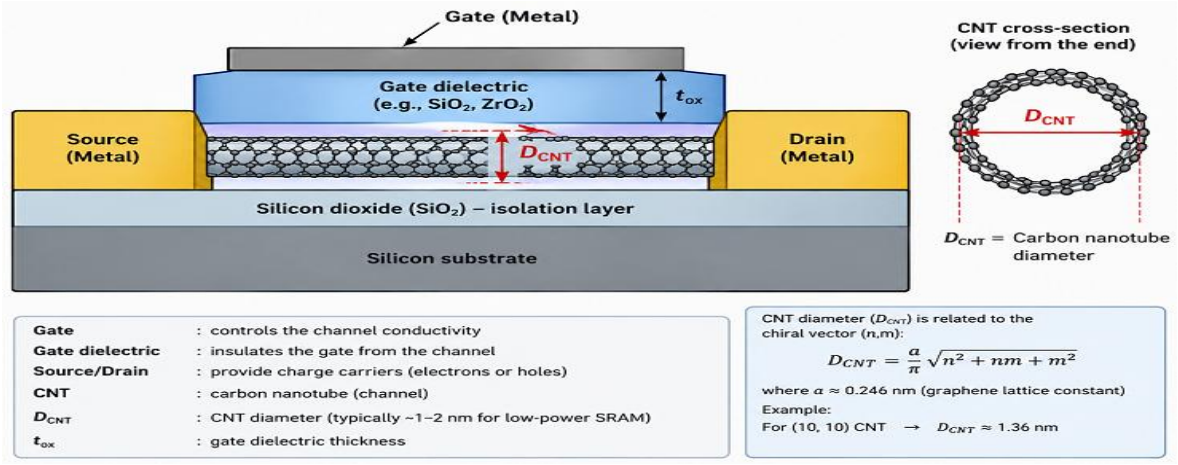


Figure 2: 2-D Structure of CNTFET (Cross-sectional View)

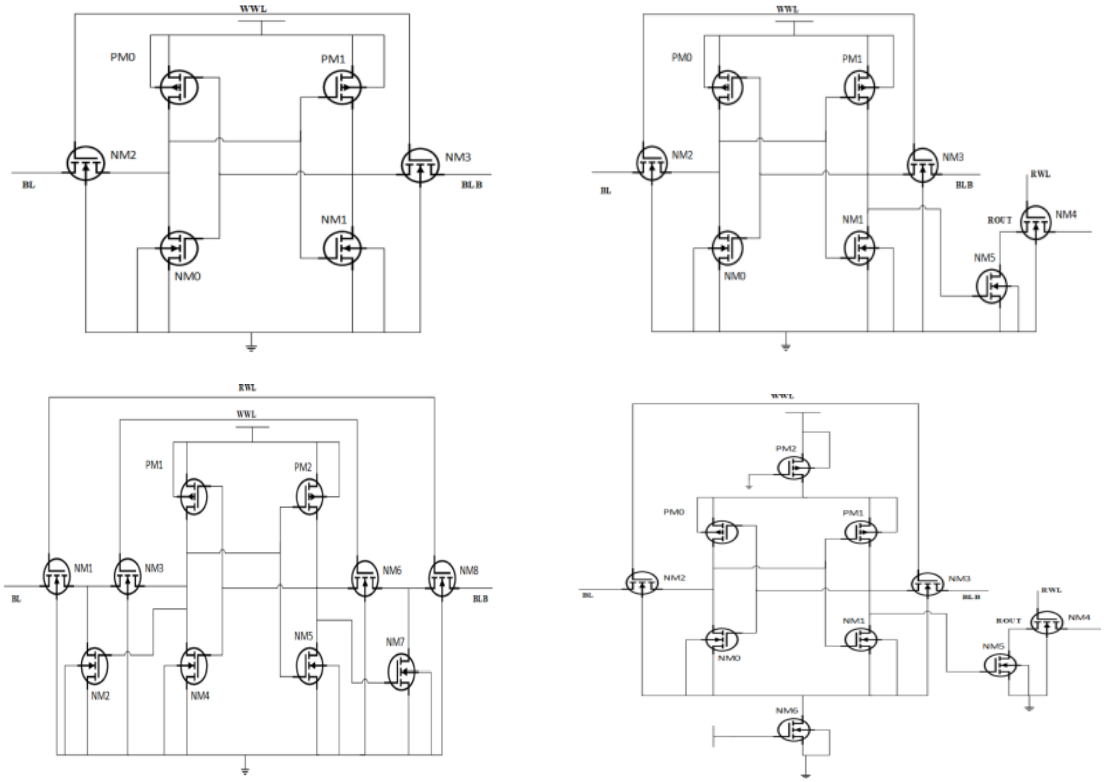


Figure 3: CNTFET Based SRAM Topologies 6T, 8T, 10T and 10 T Modified Respectively (Fuad & Nayan, 2026)

MATERIALS AND METHODS

This study is purely simulation-based and we employed a MATLAB analytical modelling to evaluate the performance of CNTFET-based SRAM cells under the variation of CNT diameter and gate-dielectric constants. Therefore, the performance of four SRAM topologies, namely 6T, 8T, conventional 10T, and modified 10T SRAM, were compared based on stability, power and delay characteristics from CNTFET Stanford-Cadence virtuoso 32 nm simulation.

Device and Material Parameters

In this work, the principal device and material parameters of the CNTFET-based SRAM cell include supply voltage, threshold voltage, CNT diameter, gate-dielectric constants, carrier mobility, oxide capacitance, quantum capacitance, effective gate capacitance, ballistic transport factor, velocity

saturation, parasitic capacitances, and load capacitance. A common device-level model was applied to the four SRAM topologies with differences in transistor count, parasitic loading, read/write paths, and circuit configuration. Table 1 shows the default values of the device and material parameters considered in the simulation.

Table 1: Default Values of the Device and Material Parameters for CNTFET Based SRAM Cells

Device Parameter	Default Value
Supply Voltage (VDD)	1.0V
Threshold voltage (Vth)	0.2203V
Channel length (Lch)	32nm
Carrier mobility exponent (m)	1.2-2.0
Carrier mobility	0.08-0.09 m^2/Vs
Fermi level (E_f)	0.6eV
Ballistic transport factor (B)	0.92
Quantum capacitance (Cq)	0.012397fF
Effective capacitance (C_{Eff})	1.6043e-16F
Parasitic capacitance (C_{Par})	0.08fF
Gate-Oxide capacitance (C_{OX})	0.065624fF
Gate-Oxide thickness (Tox)	4.0nm
Load capacitance (C_L)	0.04fF
CNT tube diameter (Dcnt)	1.0-2.0nm
Gate-dielectric Permitivity (K_{gate})	3.9-30
CNT Position /Tube's chirality	0 and 1/ (13~25, 0)

MATLAB-Based Analytical Simulation

The MATLAB-based analytical simulation was utilized to evaluate the performance of the CNTFET-based SRAM cell topologies under the variation of CNT diameter and gate-dielectric constants as follows.

The key device and material parameters of the CNTFET were all defined for all four SRAM cell topologies based on its compact model in the MATLAB editor's environment to simulate their performance through calibration and behavioral trends from Cadence Virtuoso 32nm simulation. Parametric sweeps were performed across CNT diameter (D_{CNT}) and gate-dielectric constants (k) range of approximately 1.0179-1.95575nm and 3.9-30 at respectively. The drive current and effective capacitance were estimated for all four SRAM topologies under the variation of CNT diameter and dielectric constants using Equation (5, 6 and 12). Subsequently, this establishes a device-level electrical characteristics of the SRAM cells from the on-state and off-state source-drain current.

While initially maintaining k at 3.9, the read and write delays for the SRAM topologies were calculated from their delay model Equations (drive current and effective capacitance) using Equation (17) by varying the tube diameter from 1.0179-1.95575nm. Similarly, the read and write delays were also calculated from their delay model Equations by fixing the CNT diameter at approximately 1.95575 nm and varying the dielectric constant from 3.9 to 30.

The power consumption was estimated for all four SRAM topologies from the leakage current and effective capacitance at tube diameter range of 1.0179-1.95575nm when k is maintained at 3.9 with Equation (18-23). The PDP and EDP were estimated from power consumption and delays for all SRAM topologies with k equals 3.9 and diameter range of 1.0179-1.95575nm using Equation (26 & 27). The percentage variation in delays and performance metrics were determined relative to the reference dielectric condition.

For all the four SRAM topologies, the SNM was evaluated using the mirrored voltage-transfer characteristics (VTCs) of the cross-coupled inverters generated to form a butterfly curve using Equation (29-33). This SNM determines SRAM stability by extraction through maximum-square criterion (45-degree rotation). Plots were comparatively organized for all SRAM topologies with percentage changes relative to the selected reference conditions (D_{CNT}=1.95575nm, k=3.9-30 and D_{CNT}=1.0179-1.95575nm, k=3.9) to quantify their sensitivity to CNT diameter and dielectric-constant variations using Equation (28). The SRAM topology exhibiting the most favorable performance characteristics is identified.

Finally, for all SRAM topologies, the analysis of delay, power consumption, PDP, EDP and SNM were compared with the available Cadence/Spectre simulation based on CNT diameter and dielectric constant variations with Equation (34). Where necessary, model parameters and topology-dependent correction factors were calibrated to reproduce the characteristic trends in Cadence while retaining physically meaningful relationships between device/material parameters and SRAM performance.

Performance Metrics

The performance of the CNTFET-based SRAM cell topologies was evaluated and compared on read delay, write delay, power consumption, PDP, EDP and SNM under the variation of tube diameter range of 1.0179-1.95575 nm and dielectric constants of 3.9-30. The speed, efficiency and stability of the SRAM cells are determined by the delays, power consumption, PDP, EDP and SNM respectively.

RESULTS AND DISCUSSION

This section provides the findings from the analytical evaluation of the performance of CNTFET based SRAM cell topologies with the effect of varying CNT diameter and gate-dielectric constant on delay, power consumption, energy efficiency metrics and stability.

The Analysis of Write and Read Delay of CNTFET based 8T SRAM Cell at Different Gate-dielectric Constant

The effect of varying tube diameter on the delay characteristics of CNTFET based 8T SRAM using gate-materials with dielectric constants 3.9, 11, 16, 25 and 30 is discussed as follows.

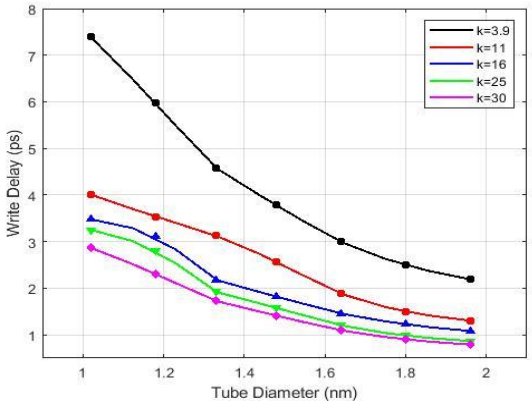


Figure 4: Write Delay Against CNT Diameter with Dielectric Constant (k)

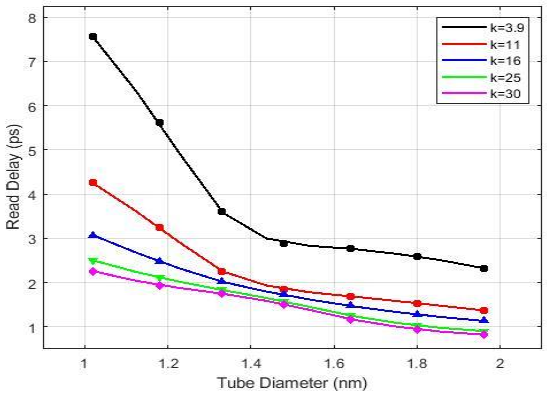


Figure 5: Read Delay Against CNT Diameter with Different Dielectric Constant (k)

Figure 4 and 5 show the effect of tube diameter on write and read delay under variation of dielectric constant. Considering hafnium silicate ($HfSiO_4$) as a dielectric material (k = 16) with CNT diameter range of 1.0179 nm to 1.95575 nm, the write and read delay decreases by 68.9% and 63.1% respectively. However, as dielectric constant ranges from 3.9 to 30 with a CNT diameter of 1.4877 nm, write and read delay decreases by 62.6% and 47.6% respectively. Therefore, the write and read delay decreases as CNT diameter increases with an improved dielectric constant value.

The Analysis of Write and Read Delay in CNTFET Based SRAM Topologies

Here, we have demonstrated the significant impact of changing tube diameter on the write and read delay of different CNTFET SRAM designs using silicon dioxide (SiO_2) as the gate-dielectric material.

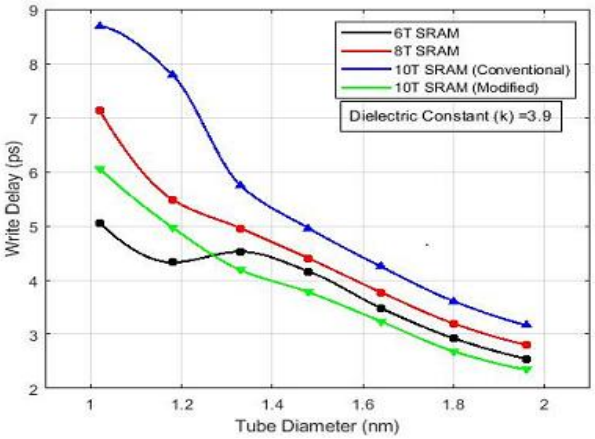


Figure 6: Write Delay Against Tube Diameter of CNTFET Based SRAM Cell Topologies

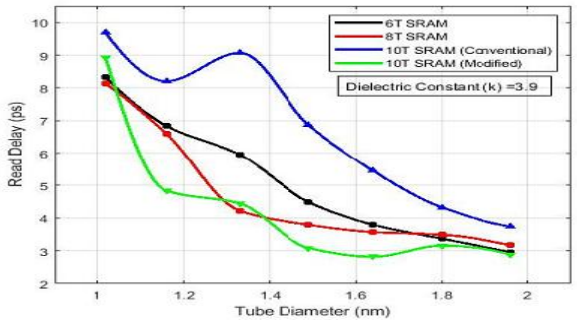


Figure 7: Read Delay Against Tube Diameter of CNTFET Based SRAM Cell Topologies

Figure 6 and 7 illustrate the significant effect of CNT diameter on delay for different types of SRAM using silicon dioxide (SiO_2) as a dielectric material (k = 3.9). When tube diameter changes from 1.0179 nm to 1.95575 nm, the write delay decreases by 49.5%, 60.6%, 63.6%, and 61.2% for 6T, 8T, 10T and 10T (modified) SRAM respectively. Under same CNT diameter range, the read delay for 6T, 8T, 10T, and 10T (modified) SRAM also reduce by 64.4%, 61.1%, 61.3%, and 67.6%, respectively. Specifically, at a tube diameter of 1.95575 nm, the write and read delay in 6T configuration is lower compared to 8T SRAM due to the presence of addition transistors. Moreover, 10T SRAM cell has an additional four transistors compared with its 6T counterpart, making its architecture more complex. Therefore, tube diameter significantly influences the switching ratio of 10T (modified) SRAM with more percentage reduction in read delay compared to write delay.

Power Consumption Analysis of CNTFET SRAM Topologies at Different Gate-dielectrics

The influence of varying tube diameter on the power consumption of CNTFET SRAM cells using different gate-materials with dielectric constants 3.9, 11, 16, 25 and 30 is highlighted as follows.

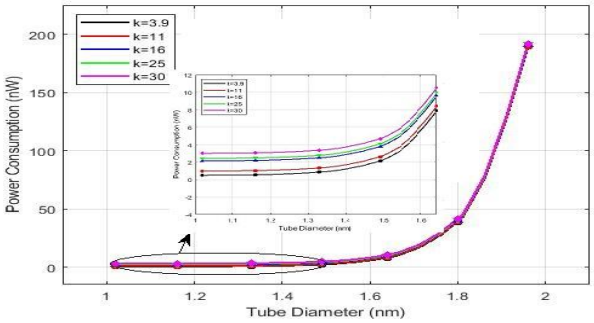


Figure 8: Power Consumption Against CNT Diameter for Different Dielectric Constant

In figure 8, the effect of CNT diameter on overall power consumption was established for different SRAM topologies using dielectric constants ranging from 3.9 to 30. The impact of tube diameter on overall power consumption of 8T CNTFET-based SRAM was demonstrated under different dielectric constants. As a result, SRAM's power consumption increases with dielectric constants. Obviously, power consumption remains almost constant with CNT diameter less than roughly 1.5 nm. However, with CNT diameter beyond 1.5 nm, power consumption rises exponentially due to an increase in leakage current. At a higher dielectric constant, the power consumption is increased with a drop in threshold voltage over an increasing tube diameter. Therefore, the overall power consumption increases by 51.4% with CNT diameter ranging from 1.0179 nm to 1.4877 nm while employing hafnium oxide (HfO_2) as the dielectric material (k = 25). Nevertheless, when the dielectric constant ranges from 3.9 to 30, with a tube diameter of 1.95575 nm there is a resulting 1.33% increase in power consumption.

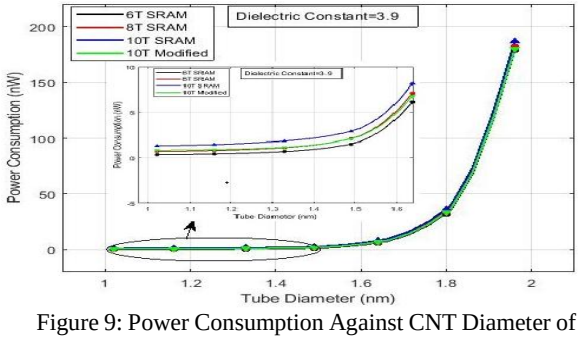


Figure 9: Power Consumption Against CNT Diameter of CNTFET Based SRAM Cell Topologies

Figure 9 shows the effect of varying tube diameter on the power consumption of different SRAM topologies. Compared to other SRAM types, 6T CNTFET-based SRAM consumes the lowest power with a value of 178.89 nW. Similarly, 10T SRAM depicts the highest power consumption with a value of 186.71 nW due to the presence of additional transistors. However, employing 10T SRAM enhances the stability of SRAM despite its potential on performance degradation.

The Analysis of the Write and Read PDP in CNTFET SRAM Topologies

The significant impact of changing tube diameter on the write and read PDP of different CNTFET SRAM designs using silicon dioxide (SiO_2) as the gate-dielectric material is discussed as follows.

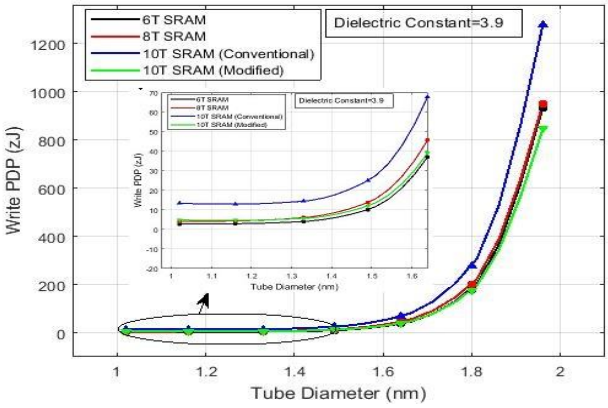


Figure 10: Write PDP Against CNT Diameter of CNTFET Based SRAM Cell Topologies

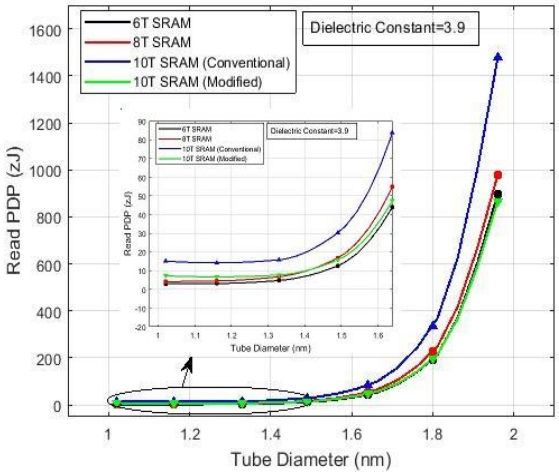


Figure 11: Read PDP Against CNT Diameter of CNTFET Based SRAM cell Topologies

Figure 10 and 11 demonstrate the trends between tube diameter and power delay product (PDP) for different SRAM topologies. At 1.0179 nm tube diameter, the write PDP values for 6 T, 8 T, 10 T, and 10 T (modified) are 2.7896 zj, 4.0681 zj, 13.4316 zj, and 4.8869 zj respectively. In the same vein, CNT diameter of 1.95575 nm estimates write PDP values of 933.3558 zj, 949.213 zj, 1277.5 zj, and 845.6461 zj for the same SRAM topologies. Furthermore, at 1.0179 nm tube diameter, the read PDP values for 6 T, 8 T, 10 T, and 10 T (modified) are 2.9338 zj, 4.1743 zj, 15.1381 zj, and 7.2686 zj, respectively. Whereas, CNT diameter of 1.95575 nm estimates read PDP values of 897.8365 zj, 979.9781 zj, 1476.70 zj, and 867.2843 zj for same SRAM topologies. Therefore, varying the tube diameter significantly impacts a greater PDP value during read operation compared to write operation.

The Analysis of the Write and Read EDP in CNTFET SRAM Topologies

This section also demonstrates the significant effect of varying tube diameter on the write and read EDP of different CNTFET SRAM designs using silicon dioxide (SiO_2) as the gate-dielectric material.

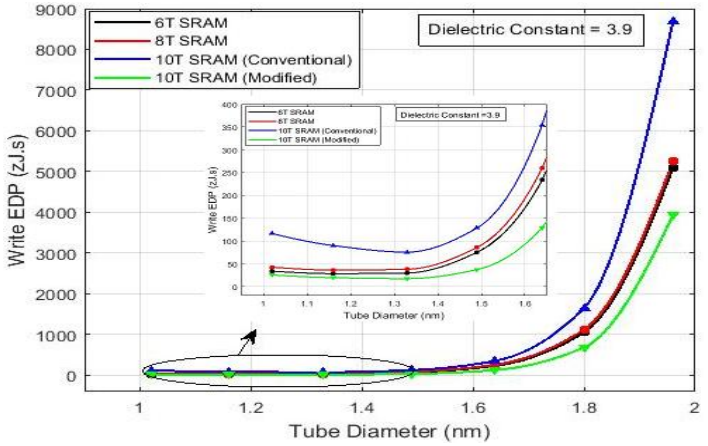


Figure 12: Write EDP Against CNT Diameter of CNTFET Based SRAM Cell Topologies

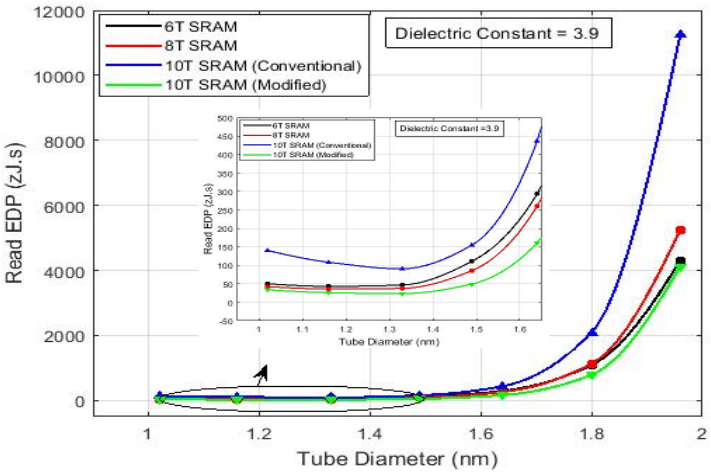


Figure 13: Read EDP Against CNT Diameter of CNTFET Based SRAM Cell Topologies

Figure 12 and 13 demonstrate the trends between tube diameter and energy delay product (EDP) for different SRAM topologies. When the tube diameter is 1.0179 nm, the write EDP values for 6 T, 8 T, 10 T, and 10 T (modified) are 33.715 zjs, 42.3617 zjs, 116.2518 zjs, and 25.3471 zjs respectively. Similarly, when the tube diameter is 1.95575 nm the write EDP values are 5088.6 zjs, 5249.5 zjs, 8682.2 zjs, and 3934.6 zjs for the same SRAM topologies. Furthermore, at 1.0179 nm tube diameter, the read EDP values for 6 T, 8 T, 10 T, and 10 T (modified) are 50.2898 zjs, 42.3617 zjs, 140.4542 zjs, and 33.8132 zjs respectively. However, at a diameter of 1.95575 nm the read EDP values are 4306.8 zjs, 5249.5 zjs, 1124.1 zjs, and 4124.7 zjs for same SRAM topologies. Therefore, varying the tube diameter significantly impacts a greater EDP value during read operation compared to write operation.

N-curve Analysis of CNTFET Based SRAM Topologies

To analyze the N-curve of CNTFET based SRAM cells, the Static Noise Margin (SNM) is considered crucial. Therefore, we determined the stability of different CNTFET SRAM cells by analyzing the SNM using 45-degree rotation method as the butterfly curve while maintaining the voltage transfer characteristics (VTCs) of their two cross-coupled inverters.

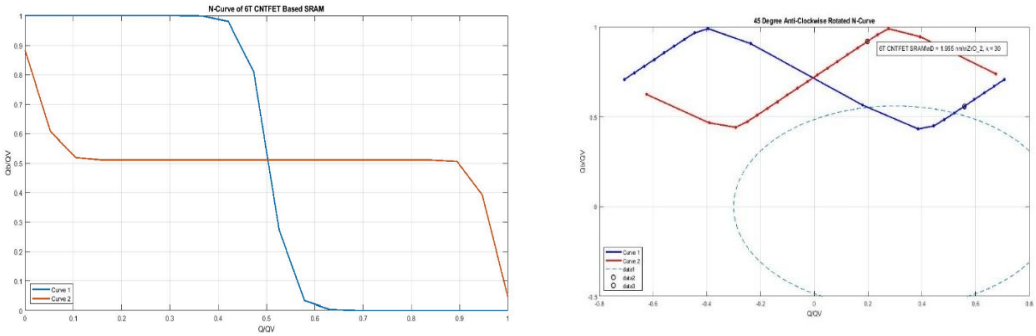


Figure 14a/14b: N-Curve of 6T CNTFET Based SRAM Using 45^0 Rotations

Figure 14a/14b illustrate the N-curve analysis of the 6 T CNTFET-based SRAM using 45-degree rotation method. This method displays the voltage transfer characteristics (VTCs) of two cross-coupled inverters which is a butterfly curve approach for estimating static noise margin (SNM). Considering a CNT diameter of approximately 1.95575 nm and Zirconium oxide (ZrO_2) as the dielectric material, the SNM for 6T SRAM is 360.62 mV. This indicates the maximum rotated separation in the lobes of the butterfly curve, which is the length of the largest square embedded within.

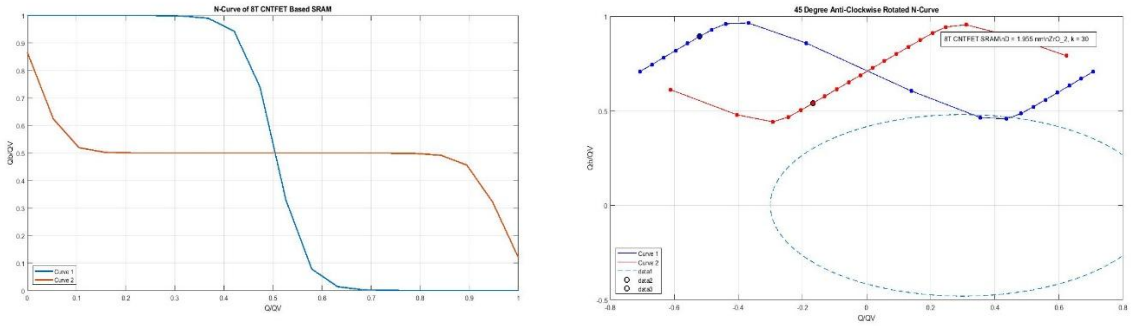


Figure 15a/15b: N-Curve of 8T CNTFET Based SRAM Using 45^0 Rotations

Similarly, figure 15a/15b demonstrate the N-curve analysis of the 8T CNTFET-based SRAM using 45-degree rotation method. Considering a CNT diameter of approximately 1.95575 nm with Zirconium oxide (ZrO_2) as the dielectric material, the SNM for 8T SRAM is 353.30 mV. Therefore, the maximum rotated separation in the lobes of the butterfly curve translates the length of the largest square embedded within as the estimated SNM.

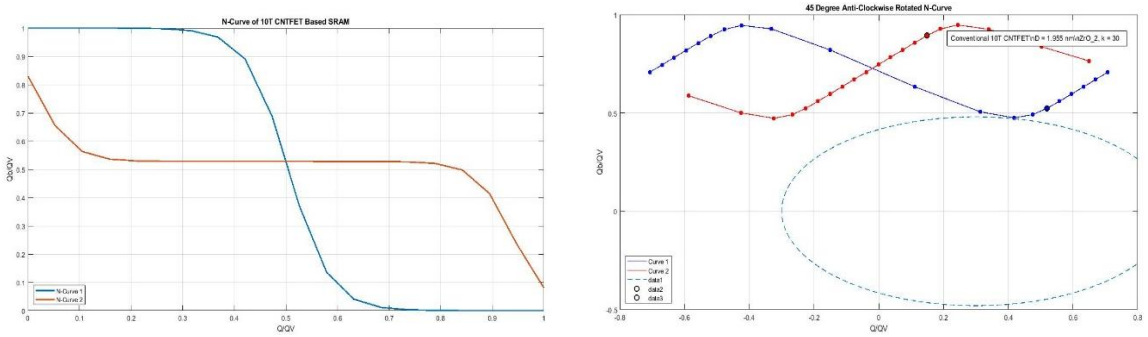


Figure 16a/16b: N-Curve of 10T CNTFET Based SRAM Using 45^0 Rotations

In figure 16a/16b, the N-curve of the 10T CNTFET-based SRAM was analyzed using 45-degree rotation method. By utilizing a CNT diameter of approximately 1.95575 nm with Zirconium oxide (ZrO_2) as the dielectric material, the SNM for 10T SRAM is 370.09 mV. This shows the maximum rotated separation within the lobes of the butterfly curve by establishing the length of the largest square embedded.

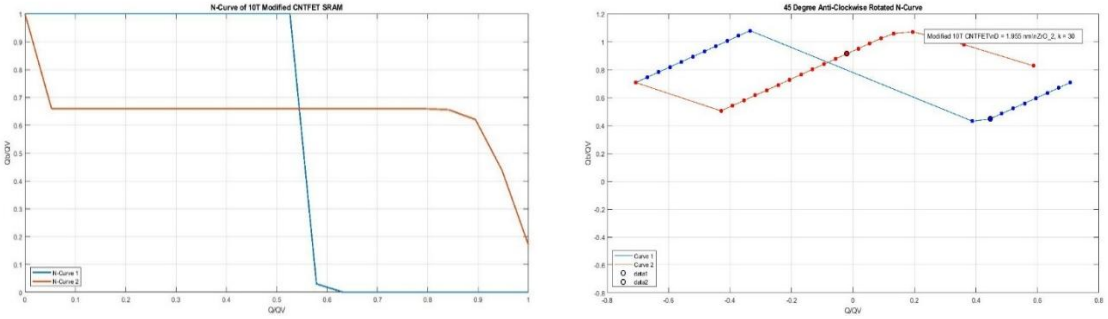


Figure 17a/17b: N-Curve of 10T (Modified) CNTFET Based SRAM Using 45^0 Rotations

Also, figure 17a/17b depict the N-curve analysis of the 10T (Modified) CNTFET-based SRAM using 45-degree rotation method. By utilizing a CNT diameter of approximately 1.95575 nm with Zirconium oxide (ZrO_2) as the dielectric material, the SNM for 10T (Modified) SRAM is 466.69 mV. As a result, the maximum rotated separation within the lobes of the butterfly curve is established which is the length of the largest square embedded. The higher the SNM value, the higher the stability of a SRAM cell. Therefore, 10T (Modified) CNTFET-based SRAM has demonstrated the highest stability compared to others due to its SNM value.

Table 2: Performance Comparison of CNTFET-Based SRAM Cells with Dielectric Constant Range of 3.9-30

Source	Technology (32nm)/ SRAM Type/Dielectric Constant (k)		Write Delay	Read Delay	Power Consumption	SNM
This Work	6T	D_{CNT}=1.0179nm	5.046ps	8.322ps	0.367nW	360.62 mV
		D_{CNT}=1.95575nm	2.549ps	2.963ps	178.888nW	
	8T	D_{CNT}=1.0179nm	7.125ps	8.138ps	0.718nW	353.30 mV
		D_{CNT}=1.95575nm	2.806ps	3.169ps	181.765nW	
	10T	D_{CNT}=1.0179nm	8.693ps	9.684ps	1.322nW	370.09 mV
		D_{CNT}=1.95575nm	3.166ps	3.745ps	186.717nW	
	10TM	D_{CNT}=1.0179nm	6.048ps	8.918ps	0.832nW	466.69 mV
		D_{CNT}=1.95575nm	2.348ps	2.8874ps	179.577nW	
	3.9	D_{CNT}=1.0179nm	7.388ps	7.556ps	0.499nW	
		D_{CNT}=1.95575nm	2.191ps	2.325ps	189.504nW	
	11	D_{CNT}=1.0179nm	4.008ps	4.253ps	0.984nW	
		D_{CNT}=1.95575nm	1.305ps	1.371ps	189.988nW	
	16	D_{CNT}=1.0179nm	3.479ps	3.073ps	2.146nW	
		D_{CNT}=1.95575nm	1.081ps	1.133ps	191.150nW	
	25	D_{CNT}=1.0179nm	3.252ps	2.504ps	2.436nW	
		D_{CNT}=1.95575nm	0.865ps	0.903ps	191.441nW	
	30	D_{CNT}=1.0179nm	2.865ps	2.259ps	3.017nw	
		D_{CNT}=1.95575nm	0.790ps	0.824ps	192.022nW	
(Fuad & Nayan, 2026)	6T	D_{CNT}=1.0179nm	5.950ps	8.600ps	0.5349nW	350.12 mV
		D_{CNT}=1.95575nm	5.250ps	4.982ps	185.1 nW	
	8T	D_{CNT}=1.0179nm	7.650ps	7.880ps	1.522nW	325.76 mV
		D_{CNT}=1.95575nm	5.350ps	5.360ps	186.92nW	
	10T	D_{CNT}=1.0179nm	8.650ps	10.15ps	1.971nW	360.85 mV
		D_{CNT}=1.95575nm	6.800ps	7.873ps	188.12nW	
	10TM	D_{CNT}=1.0179nm	6.750ps	9.820ps	2.915nW	462.21 mV
		D_{CNT}=1.95575nm	4.720ps	4.813ps	188.84nW	
	3.9	D_{CNT}=1.0179nm	7.668ps	7.900ps	0.50nW	
		D_{CNT}=1.95575nm	5.351ps	5.380ps	188.0nW	
	11	D_{CNT}=1.0179nm	5.760ps	6.120ps	1.50 nW	
		D_{CNT}=1.95575nm	5.033ps	5.050ps	190.0nW	
	16	D_{CNT}=1.0179nm	5.624ps	5.650ps	2.0 nW	
		D_{CNT}=1.95575nm	4.940ps	4.950ps	191.0nW	
	25	D_{CNT}=1.0179nm	5.502ps	5.410ps	3.0nW	
		D_{CNT}=1.95575nm	4.798ps	4.820ps	192.0nW	
	30	D_{CNT}=1.0179nm	5.360ps	5.330ps	3.3nW	
		D_{CNT}=1.95575nm	4.650ps	4.710ps	193.0nW	
(Young et al., 2008)	6T		6.3ps	7.25 ps	234.34 nW	198 mV
	8T		6.6ps	7.16 ps	448.24 nW	254 mV
(Zhang & Delgado-Frias 2012)	6T		3.06ps	29.23ps	0.185 nW	290.8 mV
	8T		2.46ps	8.96ps	0.11 nW	327.4 mV
(Valluria & Musala 2022)	6T		----	5.9ns	---	RNM=202 mV WNM=340 mV
	7T		---	3.6ns	---	RNM=223 mV WNM=360 mV
	8T		---	6.5ns	---	RNM=397 mV WNM=379mV
	9T		---	7.6ns	---	RNM=410 mV WNM=330mV
	10T		---	8.0ns	---	RNM=432mV WNM=475mV
(Pasandi et al., 2015)	10T		5.93ps	9.45ps	6.10µW	---
(Chang et al., 2009)	10T		1.0ns	6.0ns	4.9 µW	356 mV
(Kulkarni et al., 2007)	10T		13.0ps	6.0ns	3.53 µW	328 mV
(Devi et al., 2021)	8T		7.22ps	4.72ps	0.011 nW	350 mV

Table 3: Comparative Analysis of Different Technologies SRAM

Technology	Write Delay	Read Delay	Power Consumption
Homojunction TFET- 50 nm (Ahmad et al., 2019)	3.554 ns	2.929 ns	0.160 uw
Heterojunction TFET- (10 nm) (Mohammed & Chowdhury 2018)	0.346 ns	5.502 ns	3.620 nw
FinFET-(22nm) (Lakshmi & Kamaraju 2022)	98 ps	610 ps	243 nw
CNTFET-(32 nm) (Fuad & Nayan, 2026)	4.57 ps	5.775 ps	2.420 nw
CNTFET-(32 nm) This Work	1.57ps	1.89 ps	2.169 nW

Table 4: Comparative Analysis of Different Technologies SRAM

Technology	Node	SRAM type	SNM (mV)
FinFET (Rahaman & Mahapatra 2014; Rao et al., 2023)	16nm	6T/8T AUF	135.6/181.6
	32nm	6T	113
TFET (Yang et al., 2018)	32nm	7T/8T	163/170
CNTFET (Fuad & Nayan, 2026)	32nm	6T/8T/10T/10TModified	350.12/325.76/360.85/462.21
CNTFET-(32 nm) This Work	32nm	6T/8T/10T/10TModified	360.62/353.30/370.09/466.69

Table 2 shows the comparative evaluation of the MATLAB-Based analytical models against previous works at the same technology nodes. Also, table 3 and 4 highlight the improvement of our MATLAB-based analysis over other SRAM technologies at the same and different nodes. This study emphasizes the significance of MATLAB-Based analytical models on the performance of different SRAM cell topologies under CNT diameter and dielectric constant variation at 32nm simulation. Higher value of SNM and percentage reduction in read delay, write delay, power consumption and PDP and EDP was realized for the CNTFET-based SRAM cells. As shown in table 2 and 3, the performance of the proposed CNTFET-based SRAMs shows better improvement in switching speed, energy efficiency and stability due to higher SNM values, low delay, power consumption, PDP and EDP compared to other SRAM types and technologies.

CONCLUSION

In this work, the effect of CNT diameter and dielectric constant was evaluated on the performance of different CNTFET-based SRAM cell topologies using MATLAB analytical models derived from Stanford–Cadence 32 nm simulations. Relative to comparative SRAM designs, the proposed analytical framework achieved 67.6% and 61.2% reduction in read and write delay with percentage error within 15% to 50% for 10T (Modified) SRAM cell. Similarly, when the CNT diameter is maintained at 1.95575nm within a dielectric constant range of 3.9-30, reductions of 64.6% and 63.9% in read and write delay was achieved. Furthermore, there is 1.33% increase in power consumption with reductions of 63.42% in PDP and 86.8% in EDP respectively. However, while maintaining a diameter range of 1.0179-1.644nm with silicon dioxide (SiO_2) as the gate-dielectric material (k=3.9), a substantial improvement was realized while establishing 63.4% and 59.5% reduction in read and write delay respectively. In the same vein, stability increase of 2.99%, 8.45%, 2.56% and 0.97% was realized with SNM difference of 10.5mV, 27.54mV, 9.24mV and 4.48mV for 6T, 8T, 10T and 10T (modified) cells respectively. Among other SRAM topologies, 10T (modified) achieved 2.62ps delay, 856.46zJ PDP, 4029.65zJs EDP and 466.69mV SNM Value corresponding to 64.4% and 99% reduction in delay and PDP/EDP with 0.97% increase in SNM value. Overall, results demonstrate that the proposed analytical framework captures the parameter-dependent performance of CNTFET-based SRAM and provides a basis for optimizing high-speed, low-power, energy-efficient and stable nanoscale memory architectures.

Conflicts of Interest

The authors agreed to publish the work and declare no known conflict of financial interests or personal relationships that could have influenced the success of the research.

REFERENCES

Ahmad, S., Ahmad, S.A., Muqeem, M., Alam, N., & Hasan, M. (2019). TFET-based robust 7T SRAM cell for low power application. *IEEE Trans. Electron. Dev, 66* (9), 3834-3840. http://doi.org/10.1109/TED.2019.2929495

Akashe, S., Srivastava, A., & Sharma, S. (2011). Calculation of Power Consumption in 7 Transistor SRAM Cell Using Cadence Tool. *International Journal of Advances in Engineering & Technology, IJAET*, *1*(4), 189–194. Semantic Scholar Corpus ID: 18273564, ISSN: 2231-1963.

Busari, K. A., & Mutari, H. A. (2026). MATLAB-Based Performance Evaluation of an Integrated CMOS-CNTFET 8T SRAM. *Dutse Journal of Pure and Applied Sciences (DUJOPAS), 12(3d),* 392-404. https://dx.doi.org/10.4314/dujopas.v12i3d.32

Chang, I. J., Kim, J. J., Park, S. P. & Roy, K. (2009). A 32 kb 10T sub-threshold SRAM array with bit-interleaving and differential read scheme in 90 nm CMOS. *IEEE J. Solid-State Circuits. 44(2),* 650–658. https://doi.org/10.1109/JSSC.2008.2011972.

Deng, J., & Wong, H. -S. P (2007). A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application—Part I: Model of the Intrinsic Channel Region. *IEEE Transactions on Electron Devices, 54* (12), 3186-3194, http://doi.org/10.1109/TED.2007.909030

Devi, M., Madhu, C., Garg, N., Singh, S., & Singh, P. (2021). Design and Stability analysis of CNTFET based SRAM cell, *IOP Conf. Ser Mater. Sci Eng, IOP Publishing Ltd*. https://doi.org/10.1088/1757-899X/1033/1/012043.

Fei, A. (2024). A review of the development of transistor technology and its application in electronic devices. *Proceedings of the 4th International Conference on Materials Chemistry and Environmental Engineering*, *10*(2), 141–145. https://doi.org/10.54254/2755-2721/56/20240642

Fuad, M. H., & Nayan, M. F. (2026). Impact of material and structural parameters on the performance of advanced low-

power CNTFET-based SRAM designs. *www.nature.com/scientificreports*. *16:11745*, 1-21. https://doi.org/10.1038/s41598-026-47254-7.

Fuad, M. H., Noor, S. S., Nayan, M. F., & Russel, R. M. (2025a). Comprehensive analysis of CMOS and CNTFET based 8T SRAM cell. *Journal of Electronic Science and Technology*, *23*(2), 1–13. https://doi.org/10.1016/j.jnlest.2025.100306.

Fuad, M. H., Nayan, M. F., Noor, S. S., & Russel, R. M. (2025b). Comprehensive performance analysis of short-channel effects & switching speed in CNTFETs: A 2D quantum simulation approach. *Results in Engineering*, *26*, 1–18. https://doi.org/10.1016/j.rineng.2025.104513

Fuad, M. H., Noor, S. S., Hassan, K. M. M., Rahman, M., Labony, H. A. K., & Nayan, M. F. (2023). Characterizing CNTFET Logic Gate and Adder Performance Trade-offs by considering CNT Diameter and Dielectric Constant. *International Women in Engineering (WIE) Conference on Electrical and Computer Engineering (WIECON-ECE)*, 1–6. https://doi.org/979-8-3503-1965-1

Fuad, M., Yeassin, R., Raihan, A., & Mahmud, R. R. (2024). Quantum Insights into Dielectric Materials and Oxide thickness-Dependent Conductance in Single- Walled CNTFET : A Parametric Simulation Study. *International Conference on Advances in Computing, Communication, Electrical, and Smart Systems (ICACCESS)*, *8*(3), 1–7. https://doi.org/10.1109/iCACCESS61735.2024.10499571.

Gupta, R., & Dasgupta, S. (2019). Process corners analysis of data retention voltage (DRV) for 6T, 8T, and 10T SRAM cells at 45 nm. *IETE J. Res*, *65* (1), 114–119. http://doi.org/10.1080/03772063.2017.1417039.

Jahanirad, H., & Hosseini, M. (2021). An efficient reliability estimation method for CNTFET-based logic circuits. *ETRI Journal*, *43*(4), 728–745, http://doi.org/10.4218/etrij.2019-0556.

Kesavan, S. P., & Rajeswari, D. R. (2015). Australian Journal of Basic and Applied Sciences A Review of Power Consumption Analysis for SRAMs. *Australian Journal of Basic and Applied Sciences*, *9*(2), 182–192. https://doi.org/ISSN:1991-8178

Khoder B., Majdeddin A., & Led A. (2020). Impact of changing channel length and band gaps of a carbon nanotube on the current of a Carbon Nanotube Field Effect. *Al-Nahrain Journal for Engineering Sciences NJES 23(1)*, 21-29, http://doi.org/10.29194/NJES.23010021

Kulkarni, J. P., Kim, K. & Roy, K. (2007). A 160 mV robust Schmitt Trigger based subthreshold SRAM. *IEEE J. Solid-State Circuits 42(10)*, 2303–2313. https://doi.org/10.1109/JSSC.2007.897148.

Kumari, A., Rani, S., & Singh, B. (2019). Parameterized comparison of nano-transistors based on CNT and GNR materials: Effect of variation in gate oxide thickness and dielectric constant. *J. Electron. Mater. 48(5)*, 3078–3085. https://doi.org/10.1007/s11664-019-07062-4

Lakshmi, T. V., & Kamaraju, M. (2022). A review on SRAM memory design using FinFET technology. *Int. J. Syst. Dyn. Appl. 11(6)*, 1–21. https://doi.org/10.4018/IJSDA.302665.

Lázaro, A., Nae, B., Moldovan, O., & Iñiguez, B. (2006). A compact quantum model of nanoscale double-gate metal-oxide-semiconductor field-effect transistor for high frequency and noise simulations A compact quantum model of nanoscale double-gate metal-oxide-semiconductor field-effect transistor for high. *JOURNAL OF APPLIED PHYSICS*, *8*(11), 1–12. https://doi.org/10.1063/1.2360379

Liu, H., Nishide, D., Tanaka, T. & Kataura, H. (2011). Large-scale single-chirality separation of single-wall carbon nanotubes by simple gel chromatography. *Nat. Commun.* https://doi.org/10.1038/ncomms1313.

Maity, R.K., Tripathi, S., Samanta, J., & Bhaumik, J., (2020). Lower complexity error location detection block of adjacent error correcting decoder for SRAMs. *IET Comput. Digital Tech*, *14* (5), 210–216. http://doi.org/10.1049/iet-cdt.2019.0268.

Maleknejad, M., Mirzaee, R. F., Navi, K. & Dargahi, A. (2014). A systematic approach to design Boolean functions using CNFETS and an array of CNFET capacitors. *J. Circuits Syst. Comput.* https://doi.org/10.1142/S0218126614500352.

Mohammed, M. U., & Chowdhury, M. H. (2018). Reliability and energy efficiency of the tunneling transistor-based 6T SRAM cell in Sub10 nm domain. *IEEE Trans. Circuits Syst. II Express Briefs 65(12)*, 1829–1833. https://doi.org/10.1109/TCSII.2018.2874897.

Murotiya, S. L., Matta, A., & Gupta, A. (2014). Performance Evalution of CNTFET-based SRAM Cell Design. *International Journal of Electronics and Electical Engineering*, *2*(3), 200–205. https://doi.org/10.47893/IJEEE.2014.1098

Nayak, D., Acharya, D.P., Rout, P.K., & Nanda, U. (2018). A novel charge recycle read write assist technique for energy efficient and fast 20 nm 8T-SRAM array. *Solid State Electron*, *14*(8), 43–50. http://doi.org/10.1016/j.sse.2018.06.002.

Nayak, D., Rout, P.K., Sahu, S., Acharya, D.P., Nanda, U., & Tripthy, D. (2020). A novel indirect read technique-based SRAM with ability to charge recycle and differential read for low power consumption, high stability and performance. *Microelectron. Journal*, 97 104723. http://doi.org/10.1016/j.mejo.2020.104723.

Natori, K. (1994). Ballistic metal- oxide- semiconductor field effect transistor. *Journal of applied Physics. 76* (8), 4879-4890. http://doi.org/10.1063/1.357756.

Natori, K., Kimura, Y., & Shimizu, T. (2005). Characteristics of a carbon nanotube field-effect transistor analyzed as a ballistic nanowire field-effect transistor. *Journal of Applied Physics*, *97*(3), doi: https://doi.org/10.1063/1.1840096.

Nayan, M. F. (2019). Impact of Temperature on Electrical Characteristics of Ballistic Carbon Nanotube Field Effect Transistor for Different Dielectrics. *IJIREEICE*, *7*(5), 1–7, http://doi.org/10.17148/ijireeice.7501

Nidhi, D., & Prashant, D. (2019). A Review Article on Carbon Nanotube Field Effect Transistors Technology. *CSVTU Research Journal on Engineering and Technology*, *8*(1), 56–62. https://doi.org/10.30732/RJET.20190801007

Pal, S., & Islam, A. (2016). Variation tolerant differential 8T SRAM cell for ultralow power applications. *IEEE Transactions Computer Aided Design of Integrated Circuits and System*, 35(4), 549–558. http://doi.org/10.1109/TCAD.2015.2474408.

Pal, S., Bose, S., & Islam, A. (2022). Design of SRAM cell for low power portable healthcare applications. *Microsystem Technologies*, *28* (3), 833–844. http://doi: 10.1007/s00542-020-04792-z.

Pasandi, G., Jafari, M., & Imani, M. (2015). A new low-power 10T SRAM cell with improved read SNM. *Int. J. Electron.*

102(10), 1621– 1633. https://doi.org/10.1080/00207217.2014.984642.

Rahaman, M., & Mahapatra, R., (2014). "Design of a 32nm independent gate FinFET based SRAM cell with improved noise margin for low power application," *International Conference on Electronics and Communication Systems (ICECS), Coimbatore, India*, 1–5, https://doi.org/10.1109/ECS.2014.6892721.

Rao, M.V.N., Hema, M., & Raghutu, R., et al., (2023). Design and development of efficient SRAM Cell based on FinFET for low power memory applications. *Journal Electrical and Computational Engineering*, 1-8, 7069746. http://doi.org/10.1155/2023/7069746.

Rastogi, P., Dutta, T., Kumar, S., Agarwal, A., & Chauhan, Y.S. (2015). Quantum confinement effects in extremely thin body germanium n-MOSFETs. *IEEE Transactions on Electron Devices 62* (11), 3575–3580. http://doi.org/10.1108/TED.2015.2478794.

Sharma, V. K., & Kumar, A. (2025). A novel 8T SRAM cell using PFC and PPC VS-CNTFET transistor. *Journal of Engineering and Applied Science*, *72*(1), 1–21. https://doi.org/10.1186/s44147-025-00579-y

Shilpi, B., Singh, R.K., & Pattnaik, M. (2011). Static Noise Margin Analysis of Various SRAM Topologies. IACSIT International Journal of Engineering and Technology, 3(3); 304-309.

Singh, A., Jain, P., & Gupta, T.K. (2014). High Performance & Improved 8T SRAM Cell. *International Journal of Engineering Research & Technology (IJERT), 3(9),* 922-926. ISSN: 2278-0181.

Sinha, S.K., & Chaudhury, S. (2012). Oxide thickness effect on quantum capacitance in single-gate MOSFET and CNTFET devices. *Annual IEEE India Conference, INDICON*, 42–46. https://doi.org/10.1109/INDCON.2012.6420586.

Sinha, S.K., Singh, P., & Chaudhury, S. (2014). Effect of temperature and chiral vector on emerging CNTFET device, in: *International Conference on Computing for Sustainable Global Development, INDIACom IEEE Computer Society:* 432–435. https://doi.org/10.1109/IndiaCom.2014.6828174.

Sze, S. M., & Ng, K. K. (2007). Physics of Semiconductor Devices. (3rd Edition). *A JOHN WILEY & SONS, JNC.,. Hoboken, New Jersey and Canada.*

Tan, M.L.P., Lentaris, G., & Amaratunga, G. (2012). Device and circuit-level performance of carbon nanotube field-effect transistor with benchmarking against a nano-MOSFET, *Nanoscale Res. Lett.* 7 (1) 467, http://doi.org/10.1186/1556-276X-7-467.

Taur, Y., & Ning, T. H. (2013). Fundamentals of Modern " VLSI Devices. (2nd Edition). *CAMBRIDGE UNIVERSITY PRESS. New York, USA.*

Tijjani A., Galadanci G.S.M., & Babaji G. (2020). Drain Current Characteristics of Carbon-nanotube FET (CNTFET) with $SiO2$, Zr$O2$ and Hf$O2$ as Dielectric Materials using FETToy Code. *NIPES Journal of Science and Technology Research 2(2)*, 212-227, ISSN-2682-5821, https://doi.org/10.37933/nipes/2.2.2020.22.

Tiwari, M., Sharma, K.K., Rawat, L.S., & Kohli, V.C. (2015). Impact of Oxide Thickness on Gate Capacitance, Drain Current and Transconductance-A Comprehensive Analysis On MOSFET, Nanowire FET and CNTFET Devices. *International Journal for Research in Emerging Science and Technology, 2(6),* 73-85.

Valluria, A., & Musala, S. (2022). Comparative analysis of CNTFET based SRAM cells. *ECS Trans. 107,* 19177–19186. https://doi.org/10.1149/10701.19177ecst.

Yalla, A., & Nanda, U. (2019). Quasi FGMOS 6T SRAM cell design: a strategy for low power applications. *Int. J. Nanosci.*, doi: https://doi.org/10.1142/s0219581x20400049.

Yang, L., et al., (2018). "Combinational Access Tunnel FET SRAM for Ultra-Low Power Applications". *IEEE International Symposium on Circuits and Systems (ISCAS), Florence, Italy*, 1–5, https://doi.org/10.1109/ISCAS.2018.8351297.

Yang, F. et al. (2020). Chirality pure carbon nanotubes: Growth, sorting, and characterization. *Chem. Rev. 120,* 2693–2758. https://doi.org/10.1021/acs.chemrev.9b00835

Young, B K., Yong-Bin K., Fabrizio L., & Young J. L. (2008). "A low power 8T SRAM cell design technique for CNFET." *International SoC Design Conference, Busan, Korea (South), 1(1),* 176-179, https://doi.org/10.1109/SOCDC.2008.4 815601

Yuan, J., & Xue, X. (2024). Solution to SRAM static power consumption with MTCMOS. *Proceedings of the 2nd International Conference on Mechatronics and Smart Systems, 0,* 143–152. https://doi.org/10.54254/2755-2721/78/20240434

Zhang, Z., & Delgado-Frias, J. G. (2012). Carbon nanotube SRAM design with metallic CNT or removed metallic CNT tolerant approaches. *IEEE Trans. Nanotechnol. 11,* 788–798. https://doi.org/10.1109/TNANO.2012.2197636.

Zlatanov, N. (2016). *Computer Memory , Applications and Management*. *2*, 1–11. https://www.researchgate.net/publication/295550090%0D

Zhu, Q., & Qiang, Y. (2012). A survey on computer system memory management and optimization techniques. *American journal of computer architecture.* 1(3); 37-50. http://doi:10.5923/j.ajca.20120103.01.

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